Application No.: 10/089,230 Docket No.: SON-2166/SOH

(80061-0018)

AMENDMENTS TO THE CLAIMS

Please amend claim 1 as shown below and cancel claims 2, 3, 5, and 6.

- 1. (CURRENTLY AMENDED) A liquid crystal display panel comprising:
 - a plurality of source lines;
 - a plurality of gate lines;
 - an active matrix display;
 - a vertical drive circuit;
 - a first pad area;
 - a second pad area;
 - a seal area; and
- a horizontal aging circuit formed on a substrate of the liquid crystal display panel, wherein

the plurality of source lines and gate lines are laid out on the liquid crystal display panel so that the source lines and gate lines intersect,

the active matrix display having a plurality of pixels arranged at each intersection of the source lines and the gate lines such that the plurality of pixels form a matrix,

the vertical drive circuit selecting each pixel by sequentially applying scan pulses to the gate lines,

the first pad area is at a first edge portion of the substrate and is connected to a first end of each source line and to a horizontal drive circuit external to the substrate,

the second pad area is at [a] the [second] first edge portion of the substrate, wherein a pitch of the second pad area is wider than a pitch of the first pad area,

the horizontal aging circuit is at the seal area, connected to a second end of each source line, and drives all source lines by a signal propagated through a single signal line or three signal lines in response to a control signal on a control signal line, and

at least one vertical drive line is wired between the second pad area and the vertical drive circuit, and

one of the control signal line, the single signal line, and the three signal lines are wired between the second pad area and the horizontal aging circuit.

2. (CANCELED)

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3. (CANCELED)

4. (PREVIOUSLY PRESENTED) A liquid crystal panel display of claim 1, wherein the horizontal aging circuit drives each source line by a signal propagated through the single signal line or the three signal lines in response to the control signal on the control signal line via CMOS switches, NMOS switches, or PMOS switches.

Claims 5-10 are CANCELED.